CLAIMS

What is claimed is:

1. A method for reading a bit of a memory cell in a non-volatile memory (NVM) cell array, the method comprising:

providing a memory cell comprising a bit to be read and at least one other bit not to be read; and

reading said bit to be read with respect to a multi-bit reference cell, said reference cell comprising a first bit at a first non-ground programmed state and a second bit at a second non-ground programmed state.

2. The method according to claim 1, wherein said first and second programmed states of the reference cell are substantially equal.

3. The method according to claim 1, wherein said first and second programmed states of the reference cell are not equal.

4. The method according to claim 1, wherein a drain-to-source voltage (Vds) is used to read the bit to be read of the memory cell, and the method further comprises decreasing the drain-to-source voltage to obtain a current ratio greater than or equal to a predetermined amount, said current ratio being the ratio of a sensed output current of said memory cell to a current of said multi-bit reference cell used to read said memory cell.

5. The method according to claim 1, wherein said memory cell comprises a nitride read only memory (NROM) cell.